Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N/C**
2. **IN A**
3. **GND**
4. **IN B**
5. **OUT B**
6. **VDD**
7. **OUT A**
8. **N/C**

**.062”**

**.078”**

**5**

**6**

**6**

**7**

**4**

**3**

**2**

**TC4426**

**MASK**

**REF**

**NOTE: manufacturer recommends bonding pad 6 first, then pad 3, then on.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: TC4426**

**APPROVED BY: DK DIE SIZE .062” X .078” DATE: 4/27/23**

**MFG: MICRO CHIP/TELCOM THICKNESS .014” P/N: TSC4426**

**DG 10.1.2**

#### Rev B, 7/1